

MARTIN KOLLÁR

University of Technology in Košice
Department of Theory of Electrical Engineering and Measurement

A TRANSDUCER INTERFACE FOR RESISTIVE SENSOR ELEMENTS BASED ON THE USE OF A FLIP-FLOP

This paper presents a new transducer interface. This interface serves the resistive bridges. The A/D conversion is based on the use of an auto-compensatory system with two digital-to-analog converters (DACs). A new measurement technique based on the use of a flip-flop circuit is used to obtain high accuracy. The main advantages of the depicted architecture are: a) Calibration accuracy depends only on LSB and maximal differential non-linearity ($\max(DNL_1)$) of the first digital-to-analog converter (DAC). b) Resultant accuracy of measurement depends on calibration accuracy and on accuracy of the second DAC. c) Calculation of a correction formula (or look up table) and input amplifier are not required.

The experimental measurement circuit with flip-flop was constructed and simulated to verify operation of the measurement.

Keywords: Wheatstone bridge, transducer interface, self-calibration, flip-flop circuit, measurement

1. INTRODUCTION

There is, naturally, no such thing as an ideal circuit and if there were, we would quickly find out that its environment would be far from being ideal. As a result, circuits may exhibit a variety of non-ideal properties, such as noise, offset, drift, non-linear behaviour, and many others. At the same time they are affected by their ambience: many circuits show cross-sensitivities to other effects than they are supposed to sense, and their bias networks and/or leads may pick up noise and interference.

In order to be able to classify the circuit non-idealities, we have to distinguish between time-variant and time-invariant causes for deviations from the ideal behaviour, and between deterministic and statistical deviations [1]. There are different correction strategies for each of these four combinations.

In ordinary measurement systems, the inaccuracies caused by the offset and error of the gain can be eliminated by using the three-signal technique [2, 3]. To eliminate the errors caused by the non-linear behaviour, several reference signals must be applied to the measurement circuit [3]. Nowadays, specific testing methods of the ADC are based on the use of sinusoidal and triangular reference signals [4]. Correct elimination of all errors by using these methods depends mainly on the precision of these reference signals. In addition, the calculation of the correction formula or the look up table is still necessary. In high precision systems, DACs can be used to generate reference signals [3, 4]. However, reference signal generator and measurement system are usually in the same environment. Therefore, the accuracy of the reference signal generator should be at least two orders higher than desired accuracy [4].

In the proposed design, the DAC used in standard solutions for calibration, has been moved to the feedback and sensor signal from Wheatstone bridge has been processed by a flip-flop. It is so-called auto-compensatory system with a flip-flop [5]. The main advantage is in the use of the flip-flop. The following section shows that all low frequency disturbances, which are present within many locations of the flip-flop and Wheatstone bridge and all

mismatches in the elements of the flip-flop are reflected only in an offset of the flip-flop when the flip-flop is controlled with slow rising slope impulses.

2. FLIP-FLOP CIRCUIT

The circuit in Fig. 1 as the sensor based on a flip-flop circuit has been introduced in reference [6]. The standard flip-flop consisting of two transistors and two resistors (Fig. 1) is characterized by two stable states, one and zero.

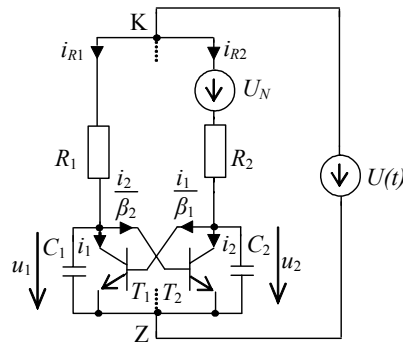


Fig. 1. Flip-flop circuit.

W. Lian and S. Middelhoek [6] proved that a flip-flop can be used for measurement of non-electrical quantities in such a way that one element of the flip-flop is replaced by a sensor. Then the principle of measurement is based on the fact that the measured non-electrical quantity breaks the value symmetry of the inverters of the flip-flop in relation to the morphological symmetry axis passing through points K and Z (Fig. 1). However, measured quantity can be compensated for by the voltage $U_N = U_{NE}$ in such a way that the 50% state is restored by repeated connection to source U . It means that the number of “ones” will be 50 % of the number of connections to voltage source [6]. The magnitude of the measured non-electrical quantity will be reflected in the voltage U_{NE} , which we will call the equivalent voltage [6, 7].

Sensing elements, which generate the voltage, can be placed within many locations of the flip-flop circuit. Wheatstone bridge can be added to the flip-flop. The flip-flop circuit with Wheatstone bridge is shown in Fig. 2a and its equivalent circuit is shown in Fig. 2b. There $U_r = U_s[R_D/(R_A+R_D)-R_C/(R_B+R_C)]$ and $R_3 = R_A||R_D+R_B||R_C$.

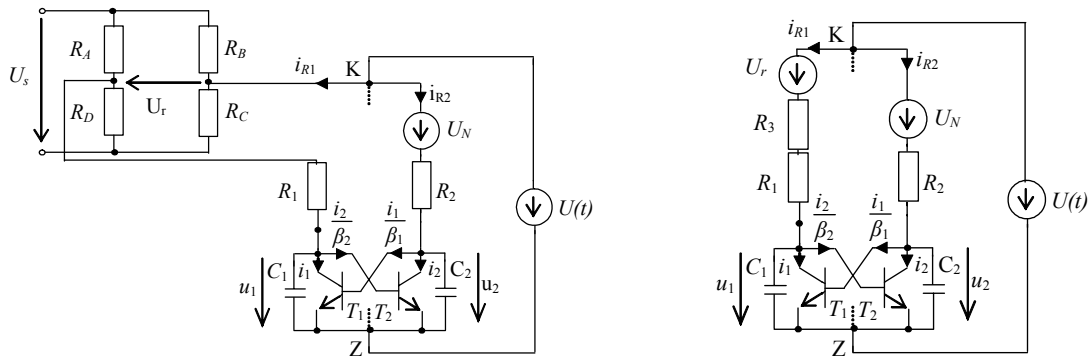


Fig. 2. Flip-flop circuit a) with Wheatstone bridge,

b) its equivalent circuit.

It should be noted that in voltage control we also distinguish between fast and slow-rising slope impulses [8, 9] (Fig. 3). The equivalent voltage can be affected by the mismatches in the capacitances of the flip-flop (Fig. 1). This can be used for measurement of the capacitances [5].

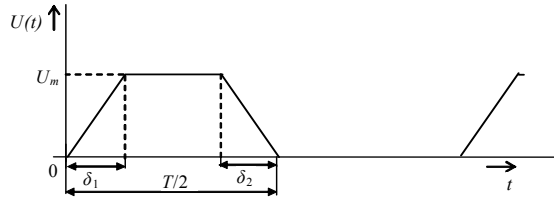


Fig. 3. Voltage control pulse.

The control by slow-rising slope impulses is characterized by such a ratio U_m/δ_1 that the currents passing through the capacitors are negligible in comparison to the transistor currents of the flip-flop. This condition is met if it is true that $\delta_1, \delta_2 > 10R_1C_1$ is at the same time $\delta_1, \delta_2 > 10R_2C_2$ [8, 9]. In the following text only control impulses with slowly rising slopes are analyzed.

2.1. State description

The flip-flop sensor, according to Fig. 2b, is described by the system of differential equations [8]

$$\frac{du_1}{dt} = \frac{R_2(U(t) - u_1 - U_r - R_1\phi_1)}{R_1R_2C_1} \equiv Q_1, \quad (1)$$

$$\frac{du_2}{dt} = \frac{R_1(U(t) - u_2 - U_N - R_2\phi_2)}{R_1R_2C_2} \equiv Q_2, \quad (2)$$

where $R_1 = R_1 + R_3$ and ϕ_1, ϕ_2 are defined as

$$\phi_1 = I_1 + \frac{I_2}{\beta_2}, \phi_2 = I_2 + \frac{I_1}{\beta_1} \quad (3)$$

and

$$I_1 = i_{ES1} e^{\frac{u_2}{V_T}}, I_2 = i_{ES2} e^{\frac{u_1}{V_T}}, \quad (4)$$

where β_1, β_2 are the current amplification coefficients, i_{ES1}, i_{ES2} are the saturation currents of bipolar transistors and V_T is a thermal voltage.

2.2. Equivalent Voltage

When, for example, one of two resistances is slightly larger than the other, the flip-flop is forced to go to a certain stable state. To qualify this effect, a DC voltage was introduced into the flip-flop sensor (as shown in Fig. 1). There exists a certain value of this voltage called the equivalent voltage at which the effect of the asymmetry in the resistors is fully compensated for by the addition of this voltage. A derivation of the magnitude of the equivalent voltage is shown in this section.

The characteristics of the flip-flop are shown in Fig. 4a. The transfer characteristic of the first inverter $u_1(u_2)$ is obtained from equation (1) with zero left side $\left(\frac{du_1}{dt} = 0\right)$. The transfer characteristic of the second inverter $u_2(u_1)$ is obtained from equation (2) with zero left side $\left(\frac{du_2}{dt} = 0\right)$. Stable and unstable states are represented by the intersection points of these characteristics. They are also called singularities in the state plane as $\frac{du_1}{dt} = 0, \frac{du_2}{dt} = 0$. One stable state is observed in Fig. 4a, if value of slowly rising impulse (Fig. 4b) is lower than certain value U_α . Two stable states 0,1 and unstable state S are observed if value of slowly rising impulse (Fig. 4b) is higher than certain value U_α . But so-called neither stable and neither unstable triple point S_p [8] is observed if value of slowly rising impulse (Fig. 4b) is equal to U_α and flip-flop is balanced by equivalent voltage U_{NE} .

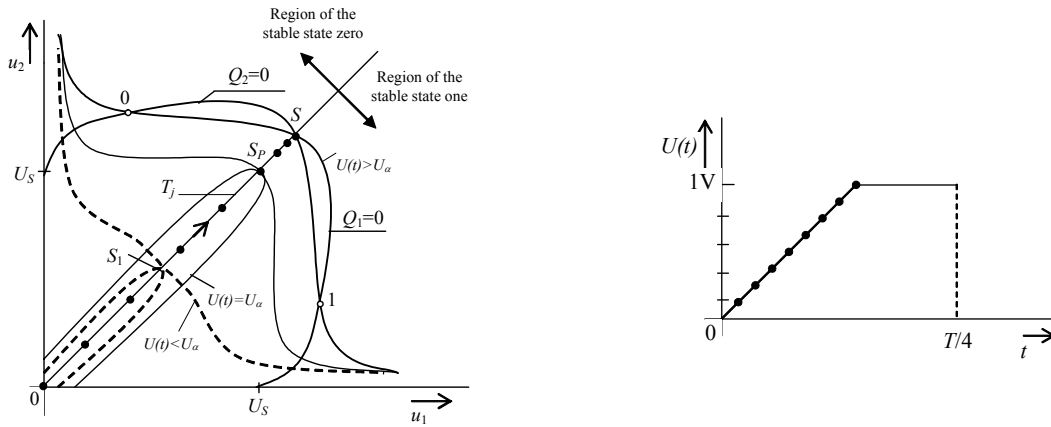


Fig. 4 a) Singularities in the state plane,

b) corresponding voltage control impulse.

Practically, the unstable state never can be achieved by the flip-flop. But taking into account a theoretical model of flip-flop, the unstable state may be assumed. Then a transition of the flip-flop into unstable state S is represented by a trajectory T_j (Fig. 4a). A boundary between the region of the stable state one and zero is also represented by this trajectory T_j . Trajectory T_j is line with a unit slope [8], which leads to

$$du_1 = du_2. \quad (5)$$

By taking the integrals of equation (5) it follows that

$$u_2 = u_1 + C, \quad (6)$$

where C is an integrating constant. As it can be seen in Fig. 3 the voltage $U(t)$ is equal to zero during the time interval $(T/2, T)$ of a control impulse. At this interval the capacitor C_2 is charged through the impulse generator and resistor R_2 on potential $-U_{NE}$ and capacitor C_1 is charged through the impulse generator and resistor R_1 on potential $-U_r$. However, the voltage U_r can change depending on the time, therefore it must hold for the frequency of a sensor signal $f < \frac{1}{R_1 C_1}$. Then with the start of the following control impulse it can be assumed that

$u_1(T) = -U_r, u_2(T) = -U_{NE}$ and from (6) we have

$$u_2 = u_1 - U_{NE} + U_r . \quad (7)$$

From the second Kirchhoff's law, of the circuit in Fig. 2a, it follows that

$$R_1 \left(I_1 + \frac{I_2}{\beta_2} + C_1 \frac{du_1}{dt} \right) + u_1 + U_r = U_{NE} + R_2 \left(I_2 + \frac{I_1}{\beta_1} + C_2 \frac{du_2}{dt} \right) + u_2 , \quad (8)$$

where currents I_1, I_2 are defined by the equation (4). Taking into account that the capacitor currents are negligible when compared to the transistor currents, by means of (7) it can be derived

$$R_1 \left(I_1 + \frac{I_2}{\beta_2} \right) = R_2 \left(I_2 + \frac{I_1}{\beta_1} \right) . \quad (9)$$

It is mentioned above, the existence of the triple point S_P is joined only with the compensation of the asymmetry of the flip-flop by equivalent voltage U_{NE} . Then the triple point is neither stable and unstable [8]. This view of the problem makes it possible to put the Jacobi matrix for given system (1), (2) relative to the treatment of the stability or instability of the given point. In case of value asymmetry let us assume $S_P = [U_1, U_2]$ so that $U_1 \neq U_2$. In order to derive Jacobi matrix from the system eq. (1), (2), the derivatives to voltage u_1 and u_2 must be taken into the triple point. Jacobi matrix is given as follows

$$\underline{J} = \begin{pmatrix} \frac{1}{R_1 C_1} \left(1 + \frac{R_1 I_2}{V_T \beta_2} \right) & \frac{I_1}{C_1 V_T} \\ \frac{I_2}{C_2 V_T} & \frac{1}{R_2 C_2} \left(1 + \frac{R_2 I_1}{V_T \beta_1} \right) \end{pmatrix} + \begin{pmatrix} \frac{1}{R_1 C_1} \frac{\partial}{\partial u_1} (U(t) - U_r(t)) & \frac{1}{R_1 C_1} \frac{\partial}{\partial u_2} (U(t) - U_r(t)) \\ \frac{1}{R_2 C_2} \frac{\partial U(T)}{\partial u_1} & \frac{1}{R_2 C_2} \frac{\partial U(T)}{\partial u_2} \end{pmatrix} , \quad (10)$$

where $I_1 = i_{ES1} e^{\frac{U_2}{V_T}}$, $I_2 = i_{ES2} e^{\frac{U_1}{V_T}}$.

Since the triple point is neither stable and unstable, the eigenvalues λ must be equal to 0. Then from

$$\det(\underline{J} - \lambda \underline{E}) = 0 \quad (11)$$

for λ equal to 0 from (7) and (9) it can be obtained

$$U_{NE} = U_r + V_T \ln \left(\frac{\left(R_1 - \frac{R_2}{\beta_1} \right) i_{ES1}}{\left(R_2 - \frac{R_1}{\beta_2} \right) i_{ES2}} \right) . \quad (12)$$

Dependence of the equivalent voltage on the output voltage from Wheatstone bridge and on the mismatches in saturation currents, load resistances and in current gains of the flip-flop can be observed from the equation (12). Note that some influences can be reflected in voltages or currents and can be found within many locations of the flip-flop circuit and the Wheatstone bridge.

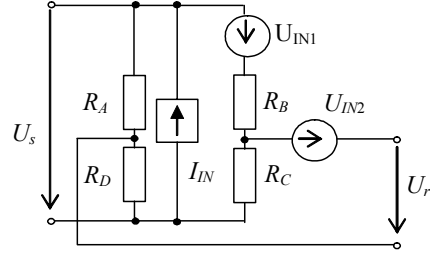


Fig. 5. Wheatstone bridge with disturbances.

The Wheatstone bridge is shown in Fig. 5. Some influences are reflected in voltage sources U_{IN1}, U_{IN2} and in current source I_{IN} . But the Wheatstone bridge is a linear circuit, which can be solved by using Thevenin's theorem. Then still a sum of contributions of voltage and current sources within the solved circuit is the result. Therefore

$$U_r' = U_r + (R_D - R_C)I_{IN} - U_{IN1} \frac{R_C}{(R_B + R_C)} - U_{IN2}, \quad (13)$$

where U_r is the non-affected voltage of the Wheatstone bridge. Conclusion is that disturbing voltage and current sources within the Wheatstone bridge are reflected only in an offset.

By using the above procedure can be shown that

$$U_{NE} = U_r(t) + V_T \ln \left(\frac{\left(R_1 - \frac{R_2}{\beta_1} \right) i_{ES1}}{\left(R_2 - \frac{R_1}{\beta_2} \right) i_{ES2}} \right) + U_d(t), \quad (14)$$

where $U_d(t)$ represents low-frequency disturbances such as a flicker noise. The resultant equation of equivalent voltage contains voltage $U_r(t)$ of Wheatstone bridge and so-called error equivalent voltage. In case that the Wheatstone bridge has a disturbance, by means of (13) it can be assumed

$$U_{NE} = U_r(t) + V_T \ln \left(\frac{\left(R_1 - \frac{R_2}{\beta_1} \right) i_{ES1}}{\left(R_2 - \frac{R_1}{\beta_2} \right) i_{ES2}} \right) + U_d(t) + (R_D - R_C)I_{IN} - U_{IN1} \frac{R_C}{(R_B + R_C)} - U_{IN2}, \quad (15)$$

where $V_T \ln \left(\frac{\left(R_1 - \frac{R_2}{\beta_1} \right) i_{ES1}}{\left(R_2 - \frac{R_1}{\beta_2} \right) i_{ES2}} \right) + U_d(t) + (R_D - R_C)I_{IN} - U_{IN1} \frac{R_C}{(R_B + R_C)} - U_{IN2}$ is a new error

equivalent voltage. It follows from eq. (15) that disturbing voltage and current sources within the Wheatstone bridge also all changes in the parameters of the flip-flop are reflected only in an offset error voltage. The equivalent does not depend on the amplitude of voltage control impulse is main advantage of using the flip-flop in comparison to an amplifier which is used in ordinary approach.

2.3. Feedback technique

It is beneficial to use a feedback technique in order to set the value of the equivalent voltage automatically. It works as follows: The output in the number of “ones” is used to generate a signal (the feedback signal). This signal is then added to the input of the flip-flop to bring the flip-flop back to the 50% position. The size of this feedback signal is a direct measure of the parameter [7].

An auto-compensatory system with the flip-flop is described in the following section.

3. PROPOSED SOLUTION

Auto-compensatory system, shown in Fig. 6, contains the following main parts:

- A flip-flop circuit to convert all causes, which can affect the value symmetry of the flip-flop, into a series of ones and zeros.
- The Wheatstone bridge as a sensing device of the flip-flop to convert a non-electrical quantity to be measured into a sensor signal U_r .
- A reversible counter 1 and a DAC 1 to compensate for the time-invariant deterministic errors and the time variant errors.
- A reversible counter 2 and a DAC 2 to measure a sensor signal of the Wheatstone bridge.
- A multiplexer to control the switching operations of the system.

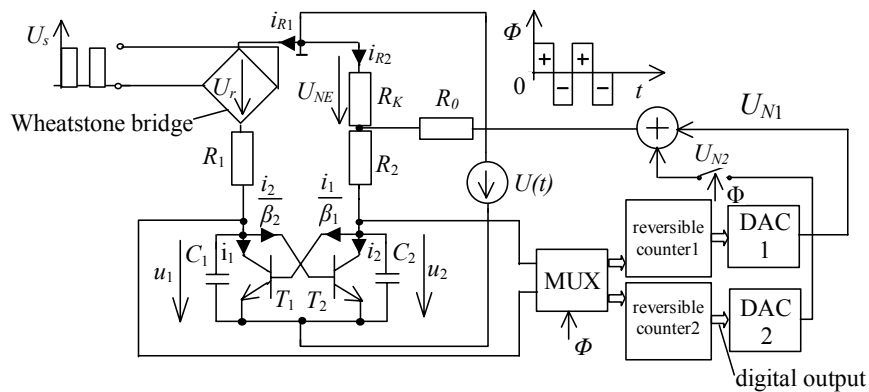


Fig. 6. Auto-compensatory system.

The idea is simple: During the first phase of a measuring cycle to compensate for the time-invariant deterministic errors and the time variant low frequency errors (supply voltage of the Wheatstone bridge is switched off), and during the second phase to measure sensor signal (supply voltage of the Wheatstone bridge is switched on). The period of the switching on and off the Wheatstone bridge is $2T$ (Fig. 3). To measure directly the sensor signal during the second phase, an adding circuit is installed to the system as it can be seen in Fig. 6. The principle of functionality, of the circuit in Fig. 6, is shown in Fig. 7. In the following text the term “disturbances and mismatches” is used for the time-invariant deterministic errors and the time variant low frequency errors.

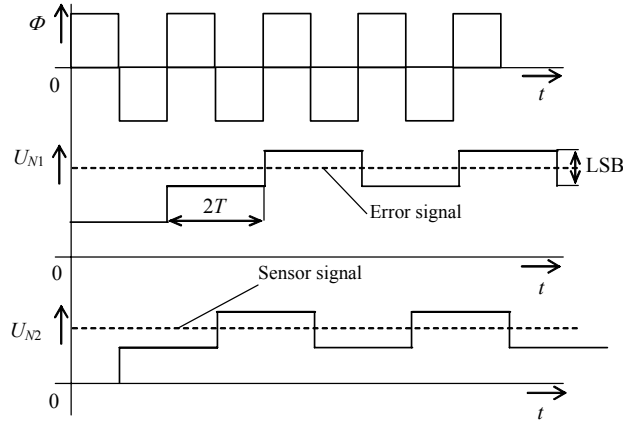


Fig. 7. The principle of system functionality.

Inaccuracy of the compensation of disturbances and mismatches is equal to $\pm 0.5 \frac{R_K}{(R_0 + R_K)} (LSB_1 + |\max(DNL_1)|)$, where $\max(DNL_1)$ is maximal differential non-linearity [4] of DAC1, and does not depend on an integral non-linearity [4] of DAC1. The absolute maximal error of measurement is given by

$$v_{\max} = \frac{R_K}{(R_0 + R_K)} \left| 0.5 (LSB_1 + |\max(DNL_1)|) + |\max(INL_2)| + 0.5 LSB_2 \right|, \quad (16)$$

where $\max(INL_2)$ is the maximal integral non-linearity of DAC2. But notice that an error of resistor-divider R_K, R_0 (Fig. 6) is not considered in (16). The value R_K usually ranges from a few Ω to tens of Ω and is at least two orders of magnitude smaller than R_0 . The resistor ratio is R_K/R_0 ($R_K \ll R_0$) and cannot be influenced by elements of the flip-flop. The value of R_K is normally four orders of magnitude smaller than R_2 . In addition, in the triple point (see Section Equivalent voltage) the equivalent resistances of the transistors of the flip-flop are a few $M\Omega$ [8]. The resistor ratio error can be derived

$$\Delta \left(\frac{R_K}{R_0} \right) = \frac{R_K}{R_0} \left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_0}{R_0} \right). \quad (17)$$

To compensate for the influence of the temperature T_h , because a thermal coefficient $\alpha = \frac{1}{R} \frac{\Delta R}{\Delta T_h}$ of a resistor R , it is sufficient to use the resistors with identical thermal coefficients. Practically, the initial resistor ratio error is about of 0.01% and resistance-ratio temperature coefficient ranges from 2 to 10 ppm/ $^{\circ}C$ [10]. The resultant absolute error is given

$$v_{\max} = \left| \Delta \left(\frac{R_K}{R_0} \right) U_r + \frac{R_K}{(R_0 + R_K)} 0.5 (LSB_1 + |\max(DNL_1)|) + |\max(INL_2)| + 0.5 LSB_2 \right| \quad (18)$$

Thus, the only dependence of measurement error on LSB and DNL of DAC1, LSB and INL of DAC2 and on resistor ratio error can be observed in (18). Since the given parameters of DAC1 and DAC2 can be changed by some influences, the error of measurement can be also

changed. However, the calibration accuracy is changed in such a way also in ordinary systems.

The other source of error that must be taken into account is error of an adding circuit (Fig. 6). But this circuit is considered in the structure for better understanding of the system functionality. Practically, the signal of DAC1 is incorporated to the first inverter of flip-flop. This modification is shown in Fig. 8.

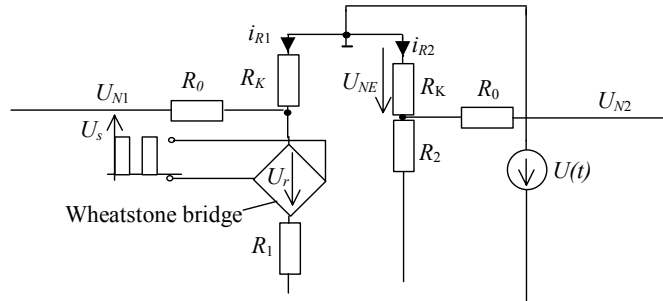


Fig. 8. Modification of auto-compensatory system.

3.1. Simulated results

The auto-compensatory system with the flip-flop was simulated in PSPICE. At the beginning, the mismatches in the load resistors of the flip-flop were assumed. The values of resistors R_1 , R_2 were changing from 7.0 to 12.0 k Ω . The remaining parameters were set as follows: $R_k = 10\Omega$, $R_0 = 1.8$ k Ω , $U_r = 0.1$ mV, $LSB = 1$ mV, $V_T = 26$ mV, $\beta_1 = \beta_2 = 100$, $i_{ES1} = i_{ES2} = 10^{-16}$ A. The flip-flop sensor was controlled by a voltage pulse according to Fig. 3, while $\delta_1, \delta_2 = 6\mu s$, $U_m = 1$ V and $T = 40\mu s$. The simulated result is shown in Fig. 9a. Corresponding error surface is shown in Fig. 9b and maximal absolute error is equal to 5.5 μV .

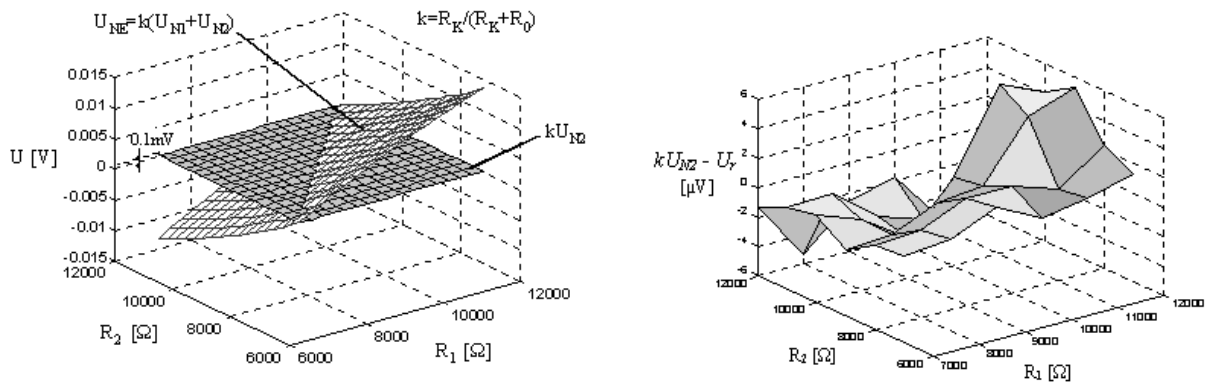


Fig. 9. a) Simulated result,

b) corresponding error surface.

Then a disturbance u_{DIS} represented by a signal $u_{DIS} = 350 \cdot 10^{-6} \sin(314t)$ was found in the flip-flop. A simulated result is shown in Fig. 10 and maximal absolute error is equal to 5 μV .

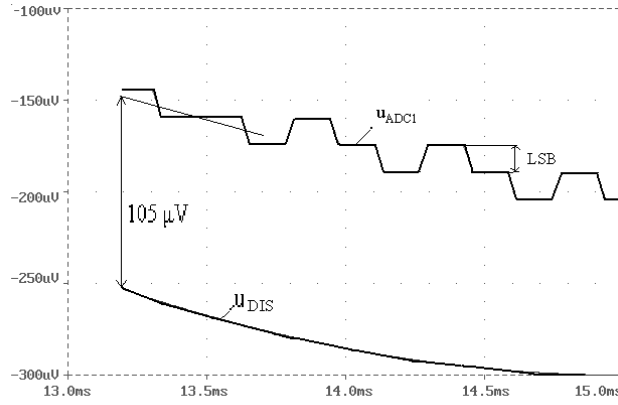


Fig. 10. Output voltage of DAC1 and a disturbing signal u_{DIS} .

3.2. Experimental results

The complete circuit was realized by using the surface montage technology. The comparators were installed between the flip-flop outputs and the reversible counters. The Wheatstone bridge as light intensity sensing element was used. The conventional resistor was substituted by photoresistor. Digital data from the reversible counter 2 were processed in PC by using LabVIEW. To verify the independence of measurement error on mismatches in the elements of the flip-flop, one of the load resistances was set to 7.0 k Ω and other resistance was subsequently given several different (from 7.0 to 12.0 k Ω). Simultaneously, the mismatch in saturation currents was simply realized by using two transistors connected in parallel on one side of the flip-flop, while on the other side, there was only one transistor. The remaining parameters were as follows: $R_k = 10\Omega$, $R_0 = 1.8\text{ k}\Omega$, $LSB = 1\text{ mV}$. The flip-flop sensor was controlled by a voltage pulse according to Fig. 3, while $\delta_1, \delta_2 = 6\mu\text{s}$, $U_m = 1\text{ V}$ and $T = 40\mu\text{s}$. The output voltage of the Wheatstone bridge was measured by a precise voltmeter to define measurement error of the auto-compensatory system. In relation to equation (18), the negligible integral and differential non-linearity leads to error one LSB . In case of this experiment it should be error 5.5 μV . But the maximal experimental error was equal to 30 μV . The reason was being looked for in the influence of a thermal and shot noise because high-frequency errors cannot be compensated for by using the auto-compensatory system (see Section Equivalent voltage). The effect of noise put on an output voltage of the DAC2 is shown in Fig. 11. Since influence of noise can be markedly eliminated by a dithering, this technique was used. The reader will find more detailed information about implementation of this method in [11]. The resultant error was compensated from 30 to 7 μV . Remaining deviation (2.5 μV) was caused by DAC1 and DAC2. Taking into account this deviation, effective number of bits (ENOB) [4] is equal to 11, because 12 bits DAC2 was used. In the following experiment a disturbing voltage U_{IN2} was employed in the Wheatstone bridge (Fig. 5). The result error was again equal to 7 μV by using the dithering.

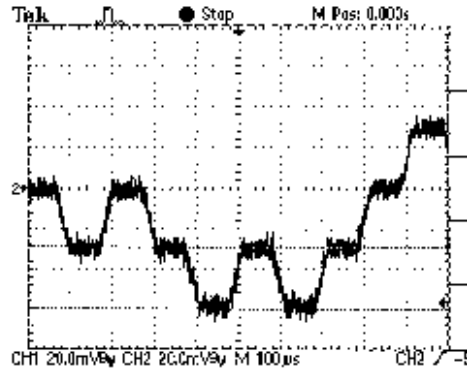


Fig. 11. Output signal of DAC2.

The aim of these experiments was to show that the error of measurement by using the auto-compensatory system with the flip-flop depends only on DAC1, 2. And from this point of view a very good agreement between experimental and simulated, theoretical results could be declared.

In the following part, dynamical properties of the auto-compensatory system will be described. From a global view, the reversible counters used in the auto-compensatory system are digital integrators. However, sensor signal of the Wheatstone bridge can be time-variant. To avoid a dynamic error it must hold

$$\left| \left(\frac{dU_r(t)}{dt} \right)_{\max} \right| < \frac{LSB}{2T}, \quad (19)$$

where T is period of the control impulses (Fig. 3). Assuming $U_r(t) = U_{rm} \sin(2\pi f_r t)$ it follows that

$$f_r < \frac{LSB}{4\pi T U_{rm}}, \quad (20)$$

where f_r is a frequency of the sensor signal.

Example: for $U_{rm} = 0.1\text{mV}$, $LSB = 1\text{mV}$, $T = 40\mu\text{s}$, according to (20), f_r will be equal to 20 kHz.

4. COMPARISON WITH THE STANDARD SOLUTIONS

The output of the Wheatstone bridge is a small differential voltage superimposed on a large common mode voltage. To provide a usable signal, an instrumentation amplifier can be used in the standard solution. The standard topology contains three operational amplifiers and seven resistors [10]. To make a comparison with the proposed solution, some basic characteristics of instrumentation amplifier are described in the following text.

The common mode rejection depends on resistor matching and overall gain. The common mode rejection ratio (CMRR) of the instrumentation amplifier is approximately equal to half resistor mismatch plus the gain. For example, a 1% resistor mismatch the CMRR is limited to 46 dB plus the gain—referred to the input. The CMRR of standard instrumentation amplifiers ranges from 65 to 120 dB. The gain stability and gain linearity also depend on the resistor matching. The gain linearity is about of 0.01% but error of gain can be ranged from 0.1 to 2%. Last characteristic that must be taken into account is an offset. Its value is at intervals from

tenths to ones of mV [10]. These errors are not trivial in high precision system. In addition, they can be markedly changed depending on some influences. Besides, the sensor signal can be affected by a time variant disturbance. A standard measuring system containing the instrumentation amplifier, ADC and calibration circuits is shown in Fig. 12.

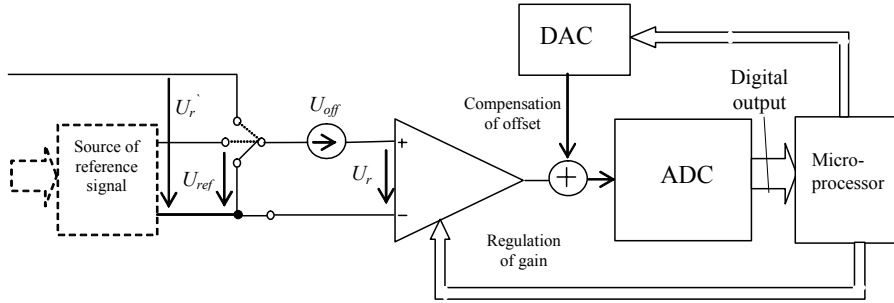


Fig. 12. Instrumentation amplifier with ADC.

Three-signal technique can be used to compensate offset and error of gain. The output voltage is given

$$U_{OUT} = (A + \Delta A)U_r + INL_{A/D}((A + \Delta A)U_r) + 0.5LSB_{A/D}, \quad (21)$$

where $INL_{A/D}$ is an integral non-linearity of ADC and ΔA is an error of gain. During the offset compensation, the inputs are short-circuited, therefore

$$U_{OUToff} = (A + \Delta A)U_{off} + INL_{A/D}((A + \Delta A)U_{off}) + 0.5LSB_{A/D}. \quad (22)$$

Then the offset compensation leads to

$$U'_{OUT} = (A + \Delta A)U_r + INL_{A/D}(U''_{OUT}) - (A + \Delta A)U_{off} - INL_{A/D}((A + \Delta A)U_{off}) - (INL_{D/A}(U_{OUToff}) + 0.5LSB_{D/A}), \quad (23)$$

where $INL_{D/A}$ is an integral non-linearity of DAC and $U''_{OUT} = (A + \Delta A)U_r - (A + \Delta A)U_{off} - INL_{A/D}((A + \Delta A)U_{off}) - (INL_{D/A}(U_{OUToff}) + 0.5LSB_{D/A})$.

The reference signal is used to compensate for error of gain, therefore

$$U_{OUTref} = U_{OUTref} - U_{OUToff} + INL_{A/D}(U''_{OUTref}) - (INL_{D/A}(U_{OUToff}) + 0.5LSB_{D/A}) + 0.5LSB_{A/D}, \quad (24)$$

where $U'_{OUTref} = (A + \Delta A)U_{ref}$ and

$U''_{OUTref} = U'_{OUTref} - U_{OUToff} - (INL_{D/A}(U_{OUToff}) + 0.5LSB_{D/A}) + 0.5LSB_{A/D}$. The error of gain, in this case, can be calculated from equation $U_{OUTref} = (A + \Delta A)U_{ref}$. From (24) it follows that

$$\Delta A = \frac{U'_{OUTref} + INL_{A/D}(U''_{OUTref}) - U_{OUToff} - (INL_{D/A}(U_{OUToff}) + 0.5LSB_{D/A}) + 0.5LSB_{A/D}}{U_{ref}} - A. \quad (25)$$

The resultant output voltage with compensation of offset and error of gain is given

$$\begin{aligned}
U_{OUT}''' &= \left((A + \Delta A) - \left(\frac{U_{OUTref}'}{U_{ref}} - A \right) \right) U_r - INL_{A/D} (U_{OUTref}'') \frac{U_r}{U_{ref}} + \\
&+ INL_{A/D} ((A + \Delta A) U_{off}) \left(\frac{U_r}{U_{ref}} - 1 \right) + \left(INL_{D/A} (U_{OUToff}) + 0.5LSB_{D/A} \right) \left(\frac{U_r}{U_{ref}} - 1 \right) + \quad (26) \\
&+ (A + \Delta A) U_{off} \left(\frac{U_r}{U_{ref}} - 1 \right) + INL_{A/D} (U_{OUT}^{IV}),
\end{aligned}$$

where

$$\begin{aligned}
U_{OUT}^{IV} &= \left((A + \Delta A) - \left(\frac{U_{OUTref}'}{U_{ref}} - A \right) \right) U_r - INL_{A/D} (U_{OUTref}'') \frac{U_r}{U_{ref}} + \\
&+ INL_{A/D} ((A + \Delta A) U_{off}) \left(\frac{U_r}{U_{ref}} - 1 \right) + \\
&+ \left(INL_{D/A} (U_{OUToff}) + 0.5LSB_{D/A} \right) \left(\frac{U_r}{U_{ref}} - 1 \right) - (A + \Delta A) U_{off} \left(\frac{U_r}{U_{ref}} - 1 \right).
\end{aligned}$$

Because $\left((A + \Delta A) - \left(\frac{U_{OUTref}'}{U_{ref}} - A \right) \right) = A$, for input signal $U_r = U_r' + U_{off}$ (Fig. 12), the resultant error is defined

$$\begin{aligned}
v &= -INL_{A/D} (U_{OUTref}'') \frac{U_r' + U_{off}}{U_{ref}} + INL_{A/D} ((A + \Delta A) U_{off}) \left(\frac{U_r' + U_{off}}{U_{ref}} - 1 \right) + \\
&+ \left(INL_{D/A} (U_{OUToff}) + 0.5LSB_{D/A} \right) \left(\frac{U_r' + U_{off}}{U_{ref}} - 1 \right) + \quad (27) \\
&+ (A + \Delta A) U_{off} \left(\frac{U_r' + U_{off}}{U_{ref}} \right) - \Delta A U_{off} + INL_{A/D} (U_{OUT}^{IV}),
\end{aligned}$$

where U_r' is sensor signal. The dependence of the resultant error of the standard system on integral non-linearity of DAC and ADC, U_{ref} and on U_{off} , according to Fig. 12, can be observed from equation (27). On the other hand, the resultant error of the measurement by using auto-compensatory system with the flip-flop, according to Fig. 6, depends only on integral and differential non-linearity of DACs. In order to show the properties of the proposed and standard solution in a more detailed way let us assume the following example: $A = 1000$, $\Delta A = 5$. DAC, also ADC, according to Fig. 12, are 12 bits. Their integral and differential non-linearity characteristics are shown in Fig. 13 and 14. These characteristics can be obtained by using standard testing methods [4, 12].

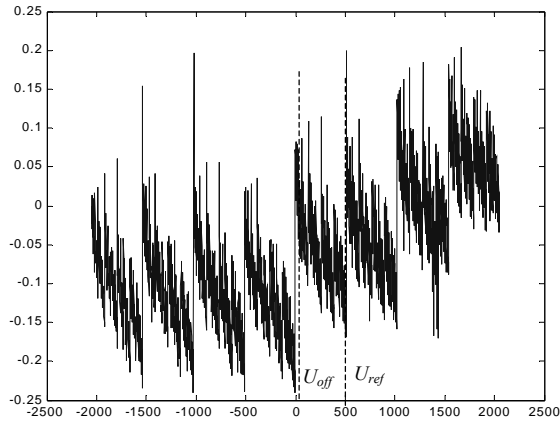


Fig. 13. Integral non-linearity as a function of output codes.

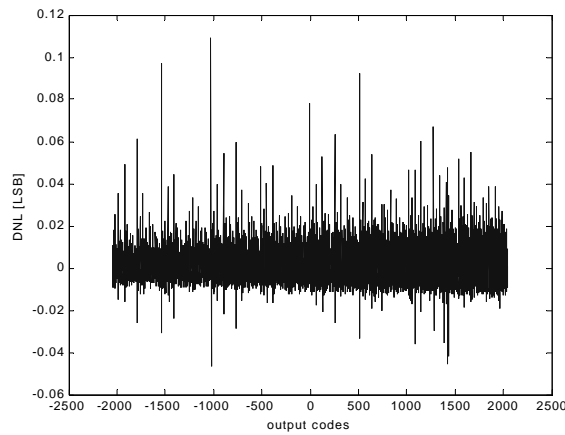


Fig. 14. Differential non-linearity as a function of output codes.

Let the values of $(A+\Delta A)U_{off}$ and U_{OUToff} correspond with output code equal to 20 and U_{OUTref} , U_{OUTref} correspond with output code equal to 500 (Fig. 13). The resultant error, according to equation (27), is shown in Fig. 15. This error ranges from -4 to 2.7 *LSB*.

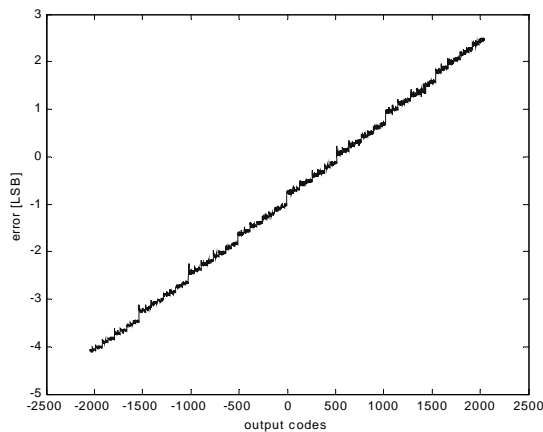


Fig. 15. Resultant error of the standard system.

However, on the other hand, the resultant error of auto-compensatory system depends only on integral and differential non-linearity of DACs (Fig. 6). The resultant error of the proposed

system, according to equation (18), is shown in Fig. 16 ($\max(DNL) = 0.11 \text{ LSB}$; Fig. 16). This error ranges from - 1.4 to 1.3 LSB and does not depend on offset and reference signal. The resistor ratio error was supposed to be equal with 0.03 %.

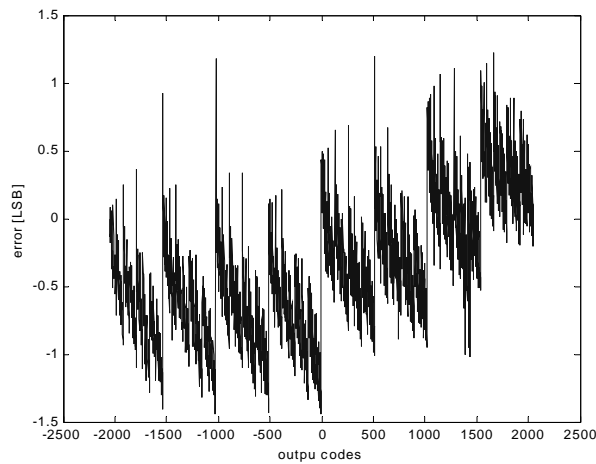


Fig. 16. Resultant error of the proposed system.

5. CONCLUSION

A transducer interface for resistive sensors has been presented. A new concept for accurate measurement has been implemented in a single circuit. In comparison to ordinary systems the type of a calibration using a precise DAC is not required. Instead two DACs are used in the feedback to compensate inaccuracies and to measure a sensor signal from the Wheatstone bridge. The main acquisition is in the use of a modified flip-flop. All disturbances and mismatches in the elements of the flip-flop and some disturbances of the Wheatstone bridge are compensated and accuracy depends only on the precision of DACs. The experimental circuit was made by surface montage technology and its immunity was being tested on extreme mismatches in elements of the flip-flop and on disturbances. ENOB of transducer interface is 11 bits by using 12 bits DAC is main test result.

ACKNOWLEDGEMENTS

This work has been supported by the Grant Agency of the Slovak Republic VEGA grant. No. 1/2180/05.

REFERENCES

1. Hosticka B.J., Brockherde W., Hammerschmidt D.: *Silicon sensors systems*. Smart sensor interfaces-Kluwer Academic Publisher, November 1997, pp. 99-111.
2. Kirianaki N. V., Yurish S. Y., Shpak N. O., Deynega V. P.: *Data Acquisition and Signal Processing for Smart Sensors*. John Willey & Sons, March 2002, p. 320.
3. Randy F.: *Understanding Smart Sensors*. Artech House, April 2000, p. 389.
4. IEEE Std. 1057-1994. IEEE Standard for digitizing waveform recorders. The institute of electrical and electronics engineers, Inc. New York, USA, 1994, p. 80.
5. Kollár M.: *Measurement of capacitances based on a flip-flop sensor*. Sensors&Transducers e-Digest (S&T), Vol. 35, No. 8-9, 2003, Toronto, Ontario – Canada, www.sensorsportal.com, p. 7.

6. Lian W., Middelhoek S.: *A new class of integrated sensors with digital output based upon the use of a flip-flop*. IEEE Electron Device Letters, Vol. EDL-7, 1986, pp. 238-240.
7. Middelhoek S., Audet S.A.: *Silicon Sensors: full of promises and pitfalls*. J.Phys. E: Sci. Instrum., Vol. 20, 1987, pp. 1080-1086.
8. Kollár, M.: *Flip-flop sensor controlled by slow-rise control pulse*. Radioengineering, Vol. 10, No. 3, 2001, pp. 34-38, ISSN 1210-2512.
9. Špány V., Pivka L.: *Dynamic properties of flip-flop sensors*, Journal of Electrical Engineering, Vol. 47, No. 7-8, p.169-178.
10. Areny P.R., Webster J.G.: *Analog signal processing*, John Wiley and sons, 1999, p. 601.
11. Kollár M.: *Uncertainty in the system for measurement of the capacitances by using flip-flop sensor*. www.electronicletters.com, Vol. 4, 2003, p. 6.
12. Arpia P., Daponte P., Michaeli L.: *Analytical a priori approach to phase-plane modeling of SAR A/D converters*. IEEE Transaction on Instrumentation and Measurement, Vol. 47, No. 4, 1998, pp. 849-857.

INTERFEJS PRZETWORNIKA DLA OPORNOŚCIOWYCH ELEMENTÓW CZUJNIKOWYCH OPARTY NA ZASTOSOWANIU PRZERZUTNIKA BISTABILNEGO.

Streszczenie

Niniejszy artykuł przedstawia nowy interfejs przetwornika. Ten interfejs jest używany z mostkami opornościowymi. Przetwarzanie analogowo-cyfrowe opiera się na użyciu systemu samokompensacyjnego z dwoma przetwornikami cyfrowo-analogowymi (D/A). Dla uzyskania dużej dokładności zastosowano nowy sposób pomiaru oparty na użyciu przerzutnika bistabilnego. Głównymi zaletami opisanej architektury są: a) Dokładność kalibracji zależy jedynie od LSB i maksymalnej nieliniowości różnicowej $\max(\text{DNL1})$ pierwszego przetwornika cyfrowo-analogowego, b) Wypadkowa dokładność pomiaru zależy od dokładności kalibracji oraz od dokładności drugiego przetwornika analogowo-cyfrowego, c) Obliczenie wzoru korekcyjnego (lub tablicy przeglądowej) i wzmacniacz wejściowy nie są wymagane.

Doświadczalny układ pomiarowy z przerzutnikiem bistabilnym został wykonany i symulowany w celu weryfikacji pomiaru.